REMARKS

The foregoing amendment does not include the introduction of new matter into the present application for invention. Therefore, the Applicant, respectfully, requests that the above amendment be entered in and that the claims to the present application be, kindly, reconsidered.

The Office Action dated September 10, 2003 has been received and considered by the Applicants. Claims 1-8 are pending in the present application for invention. Claims 1, 2, 3, and 4-8 stand rejected by the September 10, 2003 Office Action. The Office Action objects to Claim 3.

The Office Action rejects Claims 1, 2, and 4-8 under the provisions of 35 U.S.C. §102(b), as being anticipated by U.S. Patent No. 5,481,731 issued to Conary et al. (hereinafter referred to as Conary et al.). The Examiner states that Conary et al. discloses the recited elements of the rejected claims, including the first data processing unit being arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system. As support for this assertion contained within the Office action, the Examiner refers to column 19, line 60 through column 20, line 6 of Conary et al. The Applicant disagrees with this assertion contained within the Office Action. Column 19, line 60 through column 20, line 6 of Conary et al. discloses a mechanism that a processor can use to invalidate writes to the main memory that occurred during reduce power mode. As taught by Conary et al., there is a cache that belongs to the processor (see column 19, lines 60-61 of Conary et al.). Therefore, any device that writes to the main memory is not accessing the memory (the cache) belonging to the processor. Conary et al. does not disclose any mechanism for the processor to offer access to a memory that belongs to the processor. The Examiner also refers to Column 2, lines 24-29 of Conary et al., which discusses problems discusses problems associated with memory writes during a reduced power mode.

The Examiner also references column 21, lines 52-62 of Conary et al., which again discusses maintaining cache coherency between the processor cache and the external memory. Here, Conary et al., discusses the potential for invalidating individual lines within the cache. The Applicant, respectfully, submits that Conary et al. does not

disclose, or suggest, a first data processing unit offering a second data processing unit access to a memory that is dedicated to the first data processing unit during reduced power modes of operation as recited by the present invention. Accordingly, this rejection is respectfully, traversed.

Regarding Claim 2, the Examiner has quoted the same sections of Conary et al., as discussed above. Rejected Claim 2 recites that "the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a period of time in which the reduced-power mode of the data processing system implies a reduced-power mode of the first data processing unit." As discussed above, there is no "offering" from a first data processing unit to a second data processing unit of access to a memory belonging to the first data processing unit within Conary et al. Accordingly, this rejection is, respectfully traversed.

Regarding Claim 4, as previously stated, there is no "offering" of access to a memory belonging to a first data processing unit from the first data processing unit to a second data processing unit within Conary et al. Accordingly, this rejection is, respectfully traversed.

Regarding Claim 5, the Examiner states that Conary et al. on column 4, lines 61-62, discloses that the memory belonging to processor is a cache. The Applicant would like to, respectfully, point out that while Conary et al. discloses a processor with a cache, there is no disclosure, or suggestion, within Conary et al. for the cache ever to be accessed by another device. The Applicant, respectfully, submits that the simple fact that Conary et al. provides no disclose, suggestion or motivation for the processor cache to be allowed access by another device illustrates the inherent patentability of the rejected claims over Conary et al. Accordingly, this rejection is traversed.

Claim 7 is rejection as being anticipated by Conary et al. However, the wording used by the Examiner states that "it would have been obvious". There is no rejection of Claim 7 to the present invention based on obviousness. The Applicant, respectfully, asserts that the simple fact that Conary et al. includes a display within the system disclosed therein, and makes no mention, or suggestion, that a video controller can potentially be allowed access to a memory belonging to the processor, illustrates that Conary et al did not contemplate such a feature. If Conary et al. had contemplated that a video controller could access the processor's memory, there would be some mention or motivation supplied for a video controller to potentially be

allowed access to a memory belonging to the processor. There is no such disclosure or suggestion. Accordingly, this rejection is traversed.

Claim 8 is rejected in a manner similar to Claim 1 as discussed above. As discussed above, there is no disclosure, or suggestion, within Conary et al. for the processor to offer access to a memory belonging to the processor. Accordingly, this rejection is, respectfully, traversed.

The Office Action rejects Claim 8 under the provisions of 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,669,003 issued to Carmean et al. (hereinafter referred to as Carmean et al.). The Examiner states that Carmean et al. discloses a first processor offering access to a second processor or a memory dedicated to the first processor. The Applicant, respectfully, disagrees. Column 6, line 11 to column 7, line 63 of Carmean et al. does not disclose, or suggest, a processor offering access to a memory resource that is dedicated to the processor. Carmean et al. teaches steps taken after notification that a write has occurred to a dedicated memory. There is no teaching within Carmean et al. of a processor offering access to the dedicated memory. Accordingly, this rejection is, respectfully, traversed.

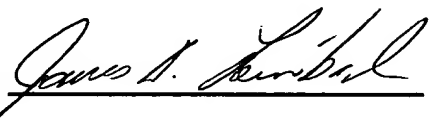
The Office Action objects to Claim 3 as being dependent upon a rejected base claim. As previously discussed, base Claim 1 is believed to be allowable.

The foregoing amendment to the claims has added new Claims 9-19 that are similar in scope to Claim 1-9 discussed above. Accordingly, new Claims 9-19 are believed to be allowable over the cited references.

Applicant is not aware of any additional patents, publications, or other information not previously submitted to the Patent and Trademark Office which would be required under 37 C.F.R. 1.99.

In view of the foregoing amendment and remarks, the Applicant believes that the present application is in condition for allowance, with such allowance being, respectfully, requested.

Respectfully submitted,

By 

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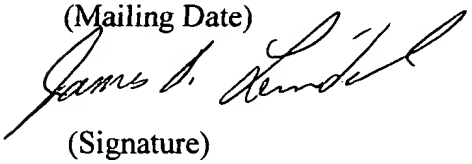

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